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10-Bit, 60 MSPS A/D Converter

PRELIMINARY DATASHEET 9/26/97 AD9051

FEATURES

- 60 MSPS Sampling Rate
- 9.3 Effective Number of Bits at fin = 10.3MHz
- 250mW Total Power at 60MSPS
- Selectable Input Bandwidth of 50 or 140 MHz
- On chip T/H and Voltage Reference
- Single +5V Supply Voltage
- Selectable +5V or 3V Logic I/O
- Input Range and Output Coding Options Available

APPLICATIONS

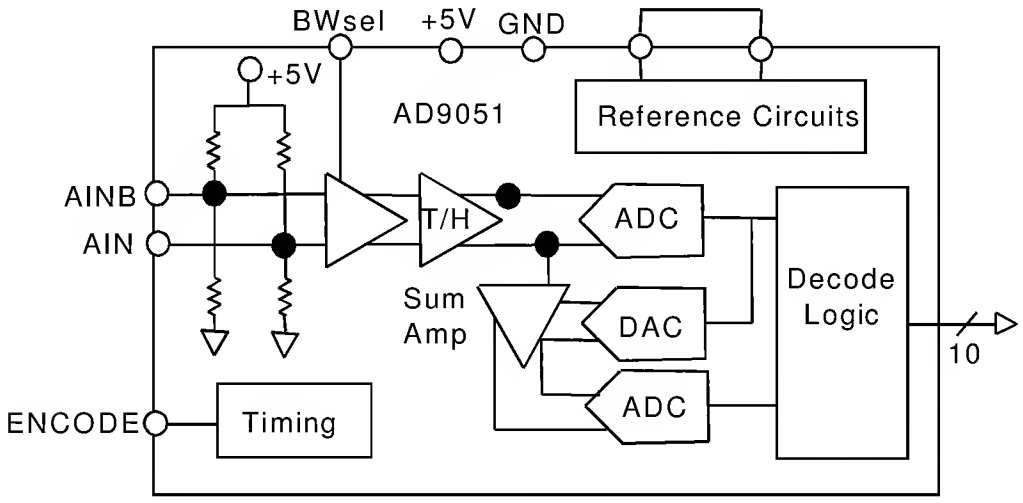
- Medical Imaging
- Digital Communications
- Professional Video
- Instrumentation
- Set Top Box

The AD9051 is a complete 10-bit monolithic sampling analog-to-digital converter (ADC) with an on-board track-and-hold and reference. The unit is designed for low cost, high performance applications and requires only +5 V and an encode clock to achieve 60 MSPS sample rates with 10-bit resolution.

The encode clock is TTL compatible and the digital outputs are CMOS; both can operate with 5 V/3 V logic, selected by the user. The two-step architecture used in the AD9051 is optimized to provide the best dynamic performance available while maintaining low power consumption.

A 2.5 V reference is included on-board, or the user can provide an external reference voltage for gain control or matching of multiple devices. Fabricated on a state of the art BiCMOS process, the AD9051 is packaged in a space saving surface mount package (SSOP) and is specified over the industrial (-40°C to +85°C) temperature range.

AD9051 Block Diagram



REV. 1

AD9051—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (VD, VDD = +5 V; external reference = 2.50V; ENCODE = 60 MSPS unless otherwise noted)

Parameter	Temp	Test Level	AD9051BRS			Units
			Min	Typ	Max	
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.75	1.50	LSB
	Full	VI		1.0		LSB
Integral Nonlinearity	+25°C	I		0.75	1.50	LSB
	Full	VI		1.0		LSB
No Missing Codes	Full	VI		Guaranteed		
Gain Error [1]	+25°C	I		±1.0	±5.0	% FS
	Full	VI		±2.5		% FS
Gain Tempco [1]	Full	V		±50		ppm/°C
ANALOG INPUT						
Input Voltage Range [2]	+25°C	V		1.25		V p-p
Input Offset Voltage	+25°C	I		5.0	±7.0	mV
	Full	VI			±25.0	mV
Input Resistance	+25°C	I	TBD	6.0	TBD	k ohms
Input Capacitance	+25°C	V		5		pF
Analog Bandwidth (BW SEL +Vd / NC) [3]	+25°C	V		50 / 140		MHz
BANDGAP REFERENCE						
Output Voltage (Io @ TBD mA)	Full	VI	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±50		ppm/°C
Power Supply Sensitivity	Full	V		TBD		mV/V
Reference Input Current (Vin = 2.50V)	Full	V			TBD	uA
SWITCHING PERFORMANCE						
Maximum Conversion Rate	+25°C	I	60			MSPS
Minimum Conversion Rate [4]	+25°C	V		< 1.0	TBD	MSPS
Aperture Delay (ta)	+25°C	V		2.5		ns
Aperture Uncertainty (Jitter)	+25°C	V		5		ps, rms
Output Valid Time (tv) [5]	Full	IV	TBD	TBD		ns
Output Propagation Delay (t_{PD}) [5]	Full	IV	5		12	ns
DYNAMIC PERFORMANCE [6]						
Transient Response	+25°C	V		10		ns
Overvoltage Recovery Time	+25°C	V		10		ns
ENOBs						
fIN = 15.0 MHz (40 / 60 MSPS)	+25°C	IV		9.3 / 9.0		ENOB
fIN = 29.0 MHz (60 MSPS)	+25°C	I		9.0		ENOB
Signal-to-Noise Ratio (SINAD)						
fIN = 15.0 MHz (40 / 60 MSPS)	+25°C	IV	56	58		dB
fIN = 29.0 MHz (60 MSPS)	+25°C	I	54	56		dB
Signal-to-Noise Ratio (without Harmonics)						
fIN = 15.0 MHz (40 / 60 MSPS)	+25°C	IV	56.5	58.5		dB
fIN = 29.0 MHz (60 MSPS)	+25°C	I	54.5	56.5		dB
2nd Harmonic Distortion						
fIN = 15.0 MHz (40 / 60 MSPS)	+25°C	IV		-69		dBc
fIN = 29.0 MHz (60 MSPS)	+25°C	I		-67	-65	dBc
3rd Harmonic Distortion						
fIN = 15.0 MHz	+25°C	IV		-75		dBc
fIN = 29.0 MHz	+25°C	I		-70	-68	dBc

ELECTRICAL CHARACTERISTICS (VD, VDD = +5 V; external reference = 2.50V; ENCODE = 60 MSPS unless otherwise noted

Parameter	Temp	Test Level	AD9051BRS Min	Typ	Max	Units
Two-Tone Intermodulation Distortion (IMD)	+25°C	V		65		dBc
Differential Phase	+25°C	V		0.1		Degrees
Differential Gain	+25°C	V		0.5		%
ENCODE INPUT						
Logic "1" Voltage	Full	VI	2.0			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			1	µA
Logic "0" Current	Full	VI			1	µA
Input Capacitance	+25°C	V		10		pF
Encode Pulse Width High (tEH)	+25°C	IV	8		TBD	ns
Encode Pulse Width Low (tEL)	+25°C	IV	8		TBD	ns
DIGITAL OUTPUTS [7]						
Logic "1" Voltage	Full	VI	4.95			V
Logic "0" Voltage	Full	VI			0.05	V
Logic "1" Voltage (3.0 V)	Full	VI	2.95			V
Logic "0" Voltage (3.0 V)	Full	VI			0.05	V
Output Coding [8]				Offset Binary		
POWER SUPPLY						
VD, VDD Supply Current	Full	VI		50	TBD	mA
Power Dissipation [9]	Full	VI		250	TBD	mW
Power Supply Rejection Ratio (PSRR) [10]	+25°C	I		±10	TBD	mV/V

NOTES
1. Gain error and gain temperature coefficient are based on the ADC only (with a fixed +2.5V external reference).
2. Contact factory or authorized sales agent for information concerning the availability of expanded input voltage range devices.
3. 3dB bandwidth with full-power input signal.
4. Minimum Conversion rate where all data sheet specifications remain stable. See Figure TBD for typical performance beyond specified limits.
5. t_V and t_{PD} are measured from the threshold crossing of the ENCODE input to 0.5V and 2.4V of the digital outputs with Vdd = 3.0V. The output ac load during test is 5pF.
6. SNR / harmonics based on an analog input voltage of –1.0 dBfs referenced to a 1.25V full–scale input range. All tests performed at 60MSPS.
7. Output voltage tests performed at Isink = TBD and Isource = TBD.
8. Contact factory or authorized sales agent for information concerning the availability of alternative output coding devices.
9. Power dissipation is measured under the following conditions: analog input =TBD Vdc at 60MSPS.
10. A change in input offset voltage with respect to a change in V_D.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9051BRS	–40°C to +85°C	RS-2
AD9051/PCB	+25°C	Evaluation Board

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS*

V_D, V_{DD} ..... +7 V
Analog Inputs ..... -1.0V to V_D+1.0V
Digital Inputs ..... -0.5V to V_D
VREF IN ..... -0.5V to V_D
Digital Output Current ..... 20 mA
Operating Temperature ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature ..... +175°C
Maximum Case Temperature ..... +150°C

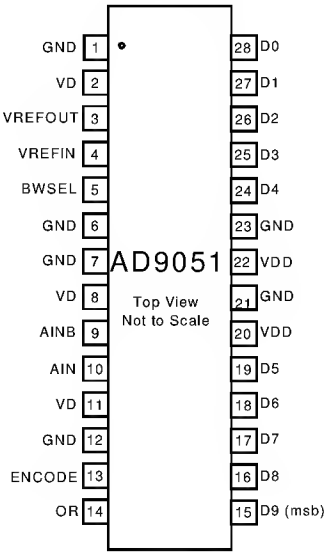
* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

AD9051 Digital Coding (Single Ended Input AIN, AINB Bypassed to GND)

Analog Input	Voltage Level	OR (Out of Range)	Digital Output MSB--------LSB
3.126	Positive Fullscale +1 LSB	1	1111111111
2.5	Midscale	0	0111111111
1.874	Negative Fullscale - 1 LSB	1	0000000000

PIN DESCRIPTIONS

Pin No.	Name	Function
1,6,7,12,21,23	GND	Ground.
2,8,11	VD	Analog +5 V power supply.
3	VREFOUT	Internal bandgap voltage reference (nominally +2.5 V)
4	VREFIN	Input to reference amplifier. Voltage reference for ADC is connected here.
5	BWSEL	Bandwidth Select. NC = 140MHz nominal. +Vd = 50MHz nominal.
9	AINB	Complimentary analog input pin (Analog input bar).
10	AIN	Analog input pin.
13	ENCODE	Encode clock input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal.
14	OR	Out of range signal. Logic "0" when analog input is in nominal range. Logic "1" when analog input is out of nominal range.
15	D9 (MSB)	Most significant bit of ADC output.
16-19	D8-D5	Digital output bits of ADC.
20,22	VDD	Digital output power supply (only used by digital outputs).
24-27	D4-D1	Digital output bits of ADC.
28	D0	Least significant bit of ADC output.



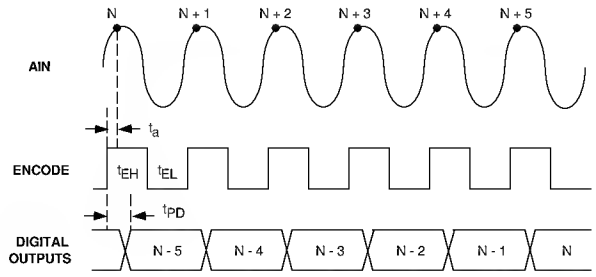
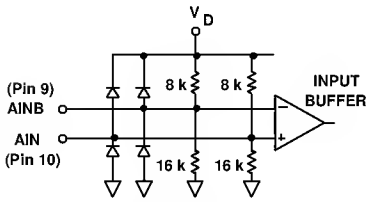
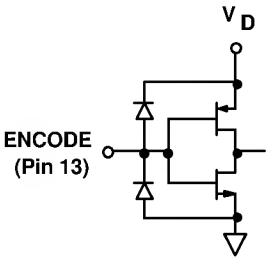


Figure 1. Timing

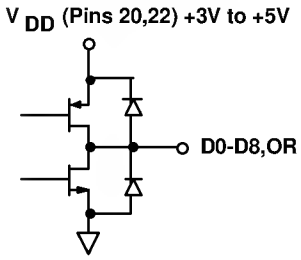
Equivalent Circuits



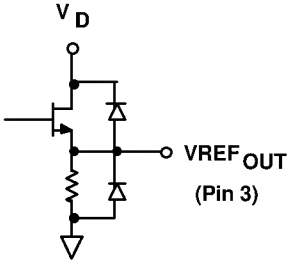
Analog Input



Encode



Output Stage



VREF

AD9051–Typical Performance Curves

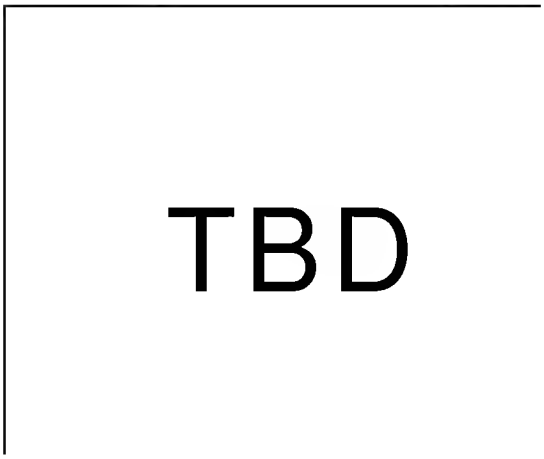


Figure X. Power Dissipation vs. Clock Rate

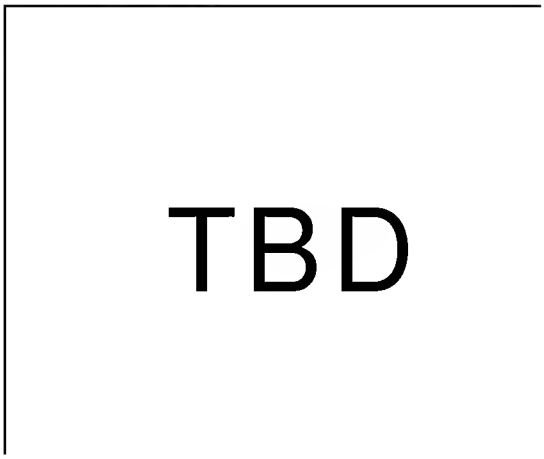


Figure X. SNR vs. Temperature

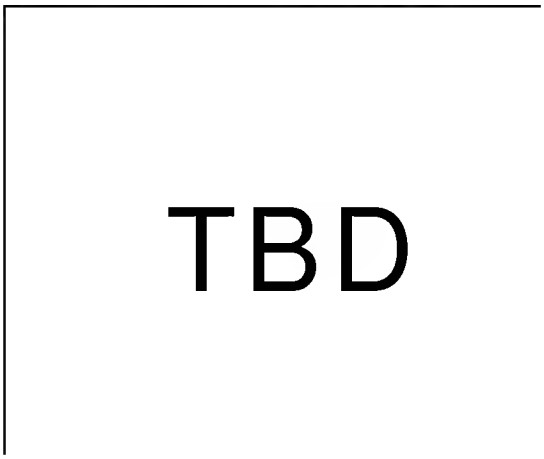


Figure X. SNR/Distortion vs. Frequency

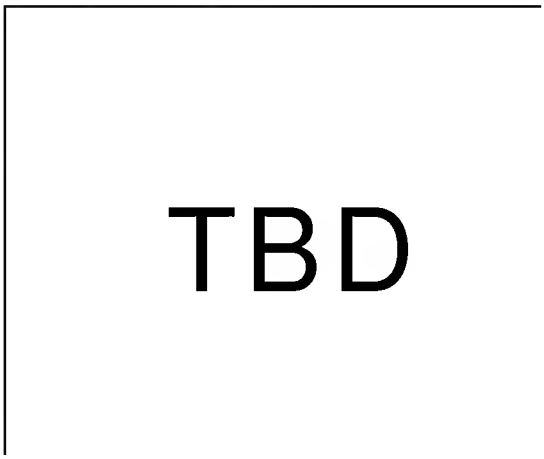


Figure X. Two-Tone IMD

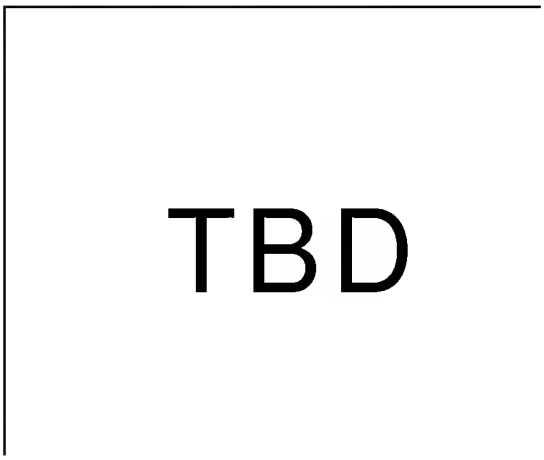


Figure X. SNR vs. Clock Rate

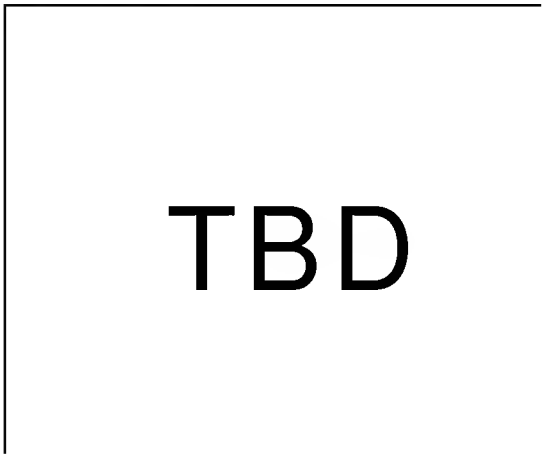


Figure X. Offset and Gain vs. Clock Rate

AD9051–Typical Performance Curves

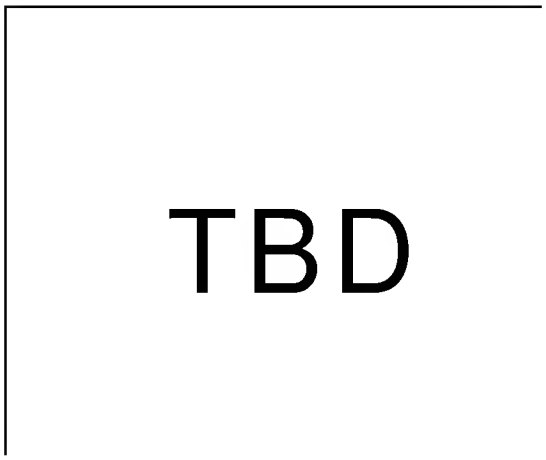


Figure X. FFT Plot 40 MSPS, 15.0 MHz

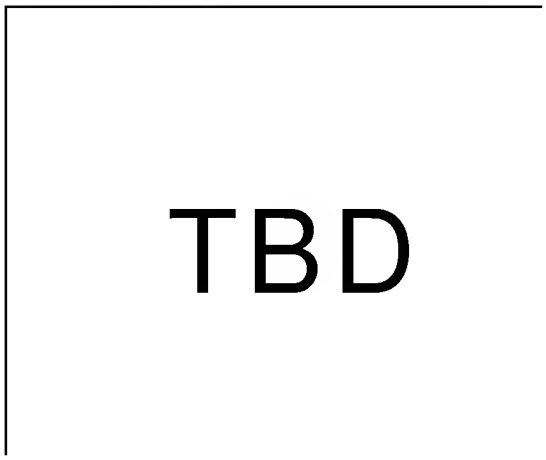


Figure X. SNR vs. Clock Pulse Width

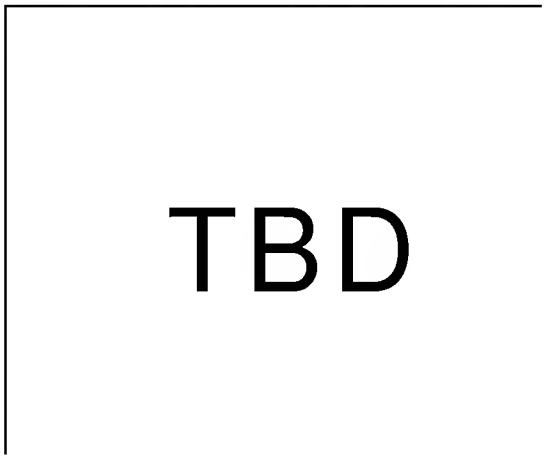


Figure X. FFT Plot 60 MSPS, 15.0 MHz

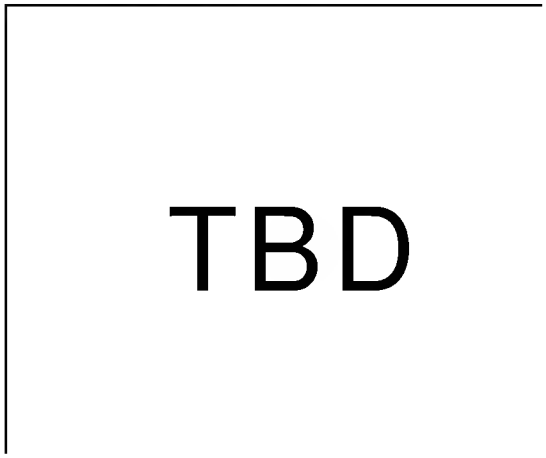


Figure X. ADC Gain vs. AIN Frequency

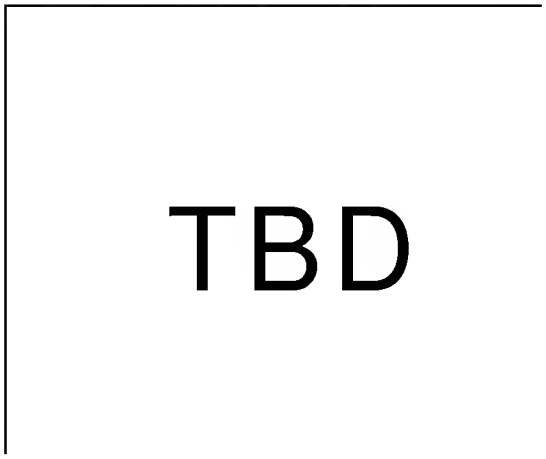


Figure X. FFT Plot 60 MSPS, 29.0 MHz

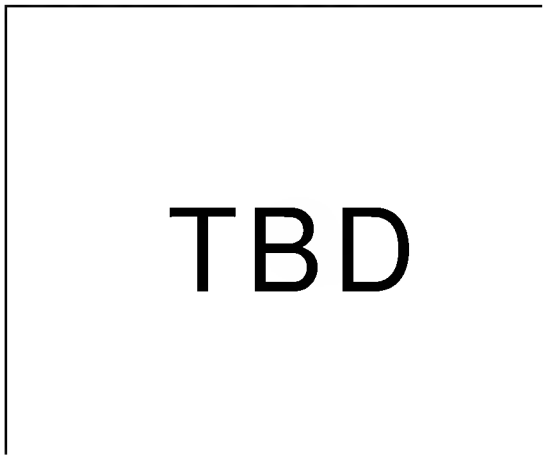


Figure X. tPD vs. Temperature 3 V/5 V

Additional Performance Curves Include

Figure X: Reference Load Regulation

Figure X: VOH / VOL vs. Sink / Source Current

THEORY OF OPERATION

Refer to the block diagram on the front page.

The AD9051 employs a subranging architecture with digital error correction. This combination of design techniques ensures true 10-bit accuracy at the digital outputs of the converter.

At the input, the analog signal is buffered by a high speed differential buffer and applied to a track-and-hold (T/H) that holds the analog value present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse. The two stage architecture completes a coarse and then a fine conversion of the T/H output signal.

Error correction and decode logic correct and align data from the two conversions and present the result as a 10-bit parallel digital word. Output data are strobed on the rising edge of the ENCODE command. The subranging architecture results in five pipeline delays for the output data. Refer to the AD9051 Timing Diagram.

USING THE AD9051

3 V System

The digital input and outputs of the AD9051 can be easily configured to directly interface to 3 V logic systems. The encode input (Pin 13) is TTL compatible with a logic threshold of 1.5 V. This input is actually a CMOS stage (refer to Equivalent Encode Input Stage) with a TTL threshold, allowing operation with TTL, CMOS and 3 V CMOS logic families. Using 3 V CMOS logic allows the user to drive the encode directly without the need to translate to +5 V. This saves the user power and board space. As with all high speed data converters, the clock signal must be clean and jitter free to prevent the degradation of dynamic performance.

The AD9051 outputs can also directly interface to 3 V logic systems. The digital outputs are standard CMOS stages (refer to AD9051 Output Stage) with isolated supply pins (Pins 20, 22 VDD). By varying the voltage on the VDD pins, the digital output levels vary respectively. By connecting Pins 20 and 22 to the 3 V logic supply, the AD9051 will supply 3 V output levels. Care should be taken to filter and isolate the output supply of the AD9051 as noise could be coupled into the ADC, limiting performance.

Analog Input

The analog input of the AD9051 is a differential input buffer (refer to AD9051 Equivalent Analog Input). The differential inputs are internally biased at +2.5 V, obviating the need for external biasing. Excellent performance is achieved whether the analog inputs are driven single-ended or differential (for best dynamic performance, impedances at AIN and AINB should match).

Figure 16 shows typical connections for the analog inputs when using the AD9051 in a dc coupled system with single ended signals. All components are powered from a single +5 V supply. The AD820 is used to offset the ground referenced input signal to the level required by the AD9051.

AC coupling of the analog inputs of the AD9051 is easily accomplished. Figure 17 shows capacitive coupling of a single ended signal while Figure 18 shows transformer coupling differentially into the AD9051.

Figure 16. Single Supply, Single Ended, DC Coupled AD9051

Figure 17. Single Ended, Capacitively Coupled AD9051

Figure 18. Differentially Driven AD9051 Using Transformer Coupling

The AD830 provides a unique method of providing dc level shift for the analog input. Using the AD830 allows a great deal of flexibility for adjusting offset and gain. Figure 19 shows the AD830 configured to drive the AD9051. The offset is provided by the internal biasing of the AD9051 differential input (Pin 9). For more information regarding the AD830, see the AD830 data sheet.

Figure 19. Level Shifting with the AD830

Overdrive of the Analog Input

Special care was taken in the design of the analog input section of the AD9051 to prevent damage and corruption of data when the input is overdriven. The nominal input range is +1.875 V to 3.125 V (1.25 V p-p centered at 2.5 V). Out-of-range comparators detect when the analog input signal is out of this range and shut the T/H off. The digital outputs are locked at their maximum or minimum value (i.e., all "0" or all "1"). This precludes the digital outputs from changing to an invalid value when the analog input is out of range.

When the analog input signal returns to the nominal range, the out-of-range comparators switch the T/H back to the active mode and the device recovers in approximately 10 ns.

The input is protected to one volt outside the power supply rails. For nominal power (+5 V and ground), the analog input will not be damaged with signals from +6.0 V to –1.0 V.

Timing

The performance of the AD9051 is very insensitive to the duty cycle of the clock. Pulse width variations of as much as ±15% for encode rates of 40 MSPS and ±8% for encode rates of 60 MSPS will cause no degradation in performance. (see Figure 13, SNR vs. Clock Pulse Width).

The AD9051 provides latched data outputs, with five pipeline delays. Data outputs are available one propagation delay (tPD) after the rising edge of the encode command

(refer to the AD9051 Timing Diagram). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9051; these transients can detract from the converter's dynamic performance.

Power Dissipation

The power dissipation specification in the parameter table is measured under the following conditions: encode is 40 MSPS or 60 MSPS, analog input is –1.0 dBFS at 10.3 MHz, the digital outputs are loaded with approximately 7 pF (10 pF maximum) and VDD is 5 V. These conditions intend to reflect actual usage of the device.

As shown in Figure 4, the actual power dissipation varies based on these conditions. For instance, reducing the clock rate will reduce power as expected for CMOS-type devices. Also the loading determines the power dissipated in the output stages. From an ac standpoint, the capacitive loading will be the key (refer to Equivalent Output Stage).

The analog input frequency and amplitude in conjunction with the clock rate determine the switching rate of the output data bits. Power dissipation increases as more data bits switch at faster rates. For instance, if the input is a dc signal that is out of range, no output bits will switch. This minimizes power in the output stages, but is not realistic from a usage standpoint.

The dissipation in the output stages can be minimized by interfacing the outputs to 3 V logic (refer to USING THE AD9051, 3 V System). The lower output swings minimize consumption. Refer to Figure 4 for performance characteristics.

Voltage Reference

A stable and accurate +2.5 V voltage reference is built into the AD9051 (Pin 3, VREF Output). In normal operation the internal reference is used by strapping Pins 3 and 4 of the AD9051 together. The internal reference has 500 µA of extra drive current that can be used for other circuits.

Some applications may require greater accuracy, improved temperature performance, or adjustment of the gain of the AD9051, which cannot be obtained by using the internal reference. For these applications, an external +2.5 V reference can be used to connect to Pin 4 of the AD9051. The VREFIN requires 5 µA of drive current.

The input range can be adjusted by varying the reference voltage applied to the AD9051. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly.

Figure 20. Evaluation Board Top Layer

Figure 21. Evaluation Board Ground Layer

Figure 22. Evaluation Board Bottom Layer

Figure 23. Silkscreen

Figure 24. Evaluation Board Schematic

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9051 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.